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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/456,873	Applicant(s) MORI, SEIICHI	
	Examiner Leonardo Andújar	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 19-32* is/are pending in the application.

4a) Of the above claim(s) *19-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. The amendment filed on 09/23/2002, paper no. 17, in response to the Office action mailed on 05/22/2002 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-8 and 19-32.

Election/Restrictions

2. Newly submitted claims 19-32 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

I. Claims 1-8, drawn to a semiconductor device, classified in class 257, subclass 314.

II. Claims 19-32, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 201.

3. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, because the device of Group I invention could be made by a process materially different from that of the Group II invention. For example, the process of claim 19 can be materially altered by using a low

pressure chemical vapor deposition (LPCVD), laser ablation or sputter deposition instead of jet vapor deposition (JVD).

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, the fields of search are not co-extensive and separate examination would be require, restriction for examination purposes as indicated is proper.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

6. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-32 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Priority

7. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/09/1998. The certified copy of the priority document has been received.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

10. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The present invention is directed to an inter insulating layer comprising a second insulating layer having a lower trap density than that of a first silicon insulating layer. However, a proper definition of trap density has not been provided. Additionally, no information or relevant literature that states the effect of the trap density in the physical or electrical properties of silicon nitride has been provided. A definition within the context of the present application is required.

11. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "an ordinary trap density obtained by typical CVD condition" in claim 5 is a relative term, which renders the claim indefinite. The phrase " a lower trap density than an ordinary trap density obtained by typical CVD" is not defined by the claim, the specification does not provide a standard for ascertaining the

requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification does not contain any disclosure regarding an actual magnitude or range of trap density typical for silicon nitride layers obtained by CVD.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

13. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Initially, and with respect to claims 1, 2 and 5 - 8 note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe

et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935). **Note that Applicant has burden of proof in such cases** as the above case law makes clear.

16. Claims 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious over Takeuchi (US 5, 907, 183).

17. Regarding claims 5 and 6 (as understood), Takeuchi (e.g. fig. 1) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate 11;
- And a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the semiconductor substrate, and a control gate 15 provided through an inter-layer insulating layer 14 on the floating gate.

18. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer contiguous to the floating gate and a silicon nitride deposited on the silicon oxide layer (col. 1/lls. 37-55). As to the grounds of rejection under section 103(a), the

method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the final device. See MPEP 2113, which discusses the handling of "product by process" claims and recommends the alternative (102 / 103) grounds of rejection.

19. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi in view of Cavins et al. (US 5,731,238).

20. Regarding claims 1 and 2, Takeuchi (e.g. fig. 9) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate;
- And a memory cell having a floating gate 23 provided through a tunnel insulating layer 22 on the semiconductor substrate, and a control gate 28 provided through an inter-layer insulating layer 71 on the floating gate.

21. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer 73 contiguous to the floating gate, a first silicon nitride 74 (conventional SiN) deposited on the silicon oxide layer and a second silicon nitride layer (col. 9/lls. 1-7). Additionally, the method for depositing the silicon nitride layers e.g. JVD, is an intermediate process step that does not affect the structure of the final device. However, Takeuchi does not disclose that the second silicon nitride layer has a lower trap density than that of the first silicon nitride layer. Cavins discloses a non volatile memory device that includes a silicon nitride (JVD) inter insulating layer 21 having a trap density lower than the conventional trap density (col.4/lls. 13-23). Moreover, Cavins discloses that this type of silicon nitride layer (JVD) is used to improve the

device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second silicon nitride layer of Takeuchi by JVD and having a lower trap density than the conventional silicon nitride trap density in order to improve the electrical performance of the device as taught by Cavins.

22. Regarding claim 2, Cavins teaches that the JVD method is performed by carrying, over a surface of thee substrate, active Si and N obtained by plasma decomposition at least a silane series gas and a gas containing nitrogen (col. 4/lls. 24-48).

23. Regarding claim 3, Cavins discloses that hydrogen quantity of a conventional silicon nitride may be more than $10^{21}/cm^3$ (col.6/lls. 23-31).

24. Regarding claim 4, Cavins discloses that hydrogen quantity of a conventional silicon nitride is close to $10^{19}/cm^3$ (col.4/lls. 15-16).

25. Regarding claims 5 and 6, Takeuchi (e.g. fig. 1) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate 11;
- And a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the semiconductor substrate, and a control gate 15 provided through an inter-layer insulating layer 14 on the floating gate.

26. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer contiguous to the floating gate and a silicon nitride deposited on the silicon oxide layer (col. 1/lls. 37-55). Takeuchi does not disclose that the silicon nitride layer is

deposited by JVD and having a lower trap density that an ordinary trap density obtained by a typical CVD. Nonetheless, Cavins discloses a non volatile memory device that includes a JVD silicon nitride inter insulating layer 21 having a trap density lower than the conventional trap density (col.4/lls. 13-23). Moreover, Cavins discloses that this type of silicon nitride layer is used to improve the device electrical performance in comparison with the conventional CVD or PECVD silicon nitride films (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second silicon nitride layer of Takeuchi by JVD (lower trap density than the conventional silicon nitride) in order to improve the electrical performance of the device as taught by Cavins.

27. Regarding claims 7 and 8, Takeuchi (e.g. fig. 1) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate 11;
- And a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the semiconductor substrate, and a control gate 15 provided through an inter-layer insulating layer 14 on the floating gate.

28. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer contiguous to the floating gate and a silicon nitride deposited on the silicon oxide layer (col. 1/lls. 37-55). Additionally, the method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the final device. However, Takeuchi does not disclose that the silicon nitride layer have a hydrogen content of $10^{19}/cm^3$ or less. Cavins discloses a non volatile memory device

that includes a silicon nitride (JVD) inter insulating layer 21 having a hydrogen content of $10^{19}/cm^3$ or less (col. 5/lls. 7-8; col. 6/lls. 27-29). Moreover, Cavins discloses that this type of silicon nitride layer (JVD) is used to improve the device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the silicon nitride layer of Takeuchi by JVD and having a hydrogen content of $10^{19}/cm^3$ or less in order to improve the electrical performance of the device as taught by Cavins.

29. Regarding claim 8, Cavins teaches that the JVD method is performed by carrying, over a surface of thee substrate, active Si and N obtained by plasma decomposition at least a silane series gas and a gas containing nitrogen (col. 4/lls. 24-48).

Response to Arguments

30. Applicant's arguments filed 09/23/2002 have been fully considered but they are not persuasive. Applicant argues that one having ordinary skills in the art would have understood adequately the meaning of the term "trap density". Applicant relies in two independent definitions (trap/density), however a concise definition of trap density was not provided. Applicant argues that one having ordinary skills in the art would have understood adequately the meaning of the term "trap density" based on the disclosure of US Patent No. 5,731,283 (Cavins). This argument is not persuasive because Cavins does not define trap density. Cavins just merely disclose a specific trap density value of a silicon nitride layer obtained by JVD (col. 4/lls. 13-19).

31. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., JVD has a trap density of less than about $1x10^{11}$ traps/cm^2 and a hydrogen concentration of less than about 10 atomic percent) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Moreover, applicant failed to proof that intermediate process step (using JVD) affects the final device structure.

32. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Cavins clearly discloses that this type of silicon nitride layer (JVD) is used to improve the device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62).

33. Applicant argues that Cavins teaches away since "a JVD silicon nitride allows one to omit the extra layers". Nonetheless, Cavins clearly teaches that the JVD silicon nitride layer can be used as a part of a gate dielectric stack or as a part of an inter-poly dielectric layer (col. 6/lls. 57-67). Therefore, the JVD silicon nitride layer disclosed by Cavins can be used alone or in combination with other layers.

34. Applicant argues that one of ordinary skill in the art would understanding adequately the limitation in issue (*i.e. an ordinary trap density obtained by a typical CVD condition*). Applicant relies on Cavins' disclosure (col. 4/lls. 13-19). Nevertheless, Cavins does not contain any disclosure regarding "an ordinary trap density obtained by a typical CVD condition". Note Cavins merely disclose a typical trap density of a JVD silicon nitride.

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

38. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

39. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/314-317, 324,325, 406, 410	11/02
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	11/02

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